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| Cases | Input (I) | Output (D) |
| A | 00000 | 00000000000000000000000000000001 |
| B | 00001 | 00000000000000000000000000000010 |
| C | 00010 | 00000000000000000000000000000100 |
| D | 00011 | 00000000000000000000000000001000 |
| E | 00100 | 00000000000000000000000000010000 |
| F | 00101 | 00000000000000000000000000100000 |
| G | 00110 | 00000000000000000000000001000000 |
| H | 00111 | 00000000000000000000000010000000 |
| I | 01000 | 00000000000000000000000100000000 |
| J | 01001 | 00000000000000000000001000000000 |
| K | 01010 | 00000000000000000000010000000000 |
| L | 01011 | 00000000000000000000100000000000 |
| M | 01100 | 00000000000000000001000000000000 |
| N | 01101 | 00000000000000000010000000000000 |
| O | 01110 | 00000000000000000100000000000000 |
| P | 01111 | 00000000000000001000000000000000 |
| Q | 10000 | 00000000000000010000000000000000 |
| R | 10001 | 00000000000000100000000000000000 |
| S | 10010 | 00000000000001000000000000000000 |
| T | 10011 | 00000000000010000000000000000000 |
| U | 10100 | 00000000000100000000000000000000 |
| V | 10101 | 00000000001000000000000000000000 |
| W | 10110 | 00000000010000000000000000000000 |
| X | 10111 | 00000000100000000000000000000000 |
| Y | 11000 | 00000001000000000000000000000000 |
| Z | 11001 | 00000010000000000000000000000000 |
| A1 | 11010 | 00000100000000000000000000000000 |
| B1 | 11011 | 00001000000000000000000000000000 |
| C1 | 11100 | 00010000000000000000000000000000 |
| D1 | 11101 | 00100000000000000000000000000000 |
| E1 | 11110 | 01000000000000000000000000000000 |
| F1 | 11111 | 10000000000000000000000000000000 |

In the 5 to 32 decoder, a signal is outputted from one of the 32 outputs which is determined by the input I. For example, if I = 11101, a signal would be outputted from D(29). This determines which of the 32 registers is accessed when writing data.